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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,044	08/25/2000	CHANDRA V. MOULI	MIO 0054 PA	6800

7590 08/05/2004

KILWORTH GOTTMAN HAGAN & SCHAEFF LLP
ONE DAYTON CENTRE SUITE 500
ONE SOUTH MAIN STREET
DAYTON, OH 45402-2023

EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,044	MOULI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 45-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 45-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 47-55 and 57 are objected to because of the following informalities: claim 47 recites the limitation "said pair of field oxide regions " in line 8. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claims 11 and 57 are objected to because of the following informalities: The term "throughbores" should read "through-holes".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 47-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of all remaining portions of said gate oxide layer between said pair of field oxide regions, as recited in claim 47, is unclear whether the pair of field oxide regions is the pair of field isolation regions

The claimed limitation of a semiconductor layer further comprises a source region and a drain region, as recited in dependent claim 56, is unclear whether the "further comprises a source region and a drain region" are the same source and drain regions recited in independent claim 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 45, 47, 49-53 and 55, insofar as in compliance with 35USC§112, are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akram et al. (WO99 31732A).

Akram teaches in figures 9 and 10 and related text a circuit structure comprising a semiconductor layer 12; a source region and a drain region 38, 40 in the semiconductor layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions;

a gate oxide layer 16e, 16f located on a surface of the channel region; and

a gate electrode 20 comprising polysilicon and one or more additional layers 22 selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having first and second leading edges located on a portion of the gate oxide layer,

where a portion of the gate oxide layer defines a first overlap region which is beneath the gate electrode and adjacent the first leading edge and inward of the second leading edge and a second overlap region of the oxide laver located beneath said gate structure and adjacent said first overlap region and said second leading edge and adjacent the drain region, the overlap region comprising fluorine having an ion implant

concentration higher than in said second overlap region and all remaining oxide layer portions extending outwardly from both the first and second leading edges of the gate structure, and which can be effective to lower the surface electrical field in the overlap region, and including a pair of spaces 44e, 44f adjacent the gate electrode.

Regarding claim 47, Akram teaches a channel region between a pair of filed isolation regions 14, wherein all remaining gate oxide layer portions extending between said pair of filed isolation regions.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 3 and 5-9 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akram et al. (WO99 31732A).

Akram teaches in figures 9 and 10 and related text a circuit structure comprising a semiconductor layer 12; a source region and a drain region 38, 40 in the semiconductor layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions;

a gate oxide layer 16e, 16f located on a surface of the channel region; and

a gate electrode 20 comprising polysilicon and one or more additional layers 22 selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having first and second leading edges located on a portion of the gate oxide layer,

where a portion of the gate oxide layer defines a first overlap region which is beneath the gate electrode and adjacent the first leading edge and inward of the second leading edge and a second overlap region of the oxide laver located beneath said gate structure and adjacent said first overlap region and said second leading edge and adjacent the drain region, the overlap region comprising fluorine having an ion implant concentration higher than in said second overlap region and all remaining oxide layer portions extending outwardly from both the first and second leading edges of the gate structure, and which can be effective to lower the surface electrical field in the overlap region, and including a pair of spaces 44e, 44f adjacent the gate electrode.

Akram does not explicitly state that the fluorine is effective to lower the surface electrical field in the overlap region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use fluorine in Akram's device sufficient to

lower the surface electrical field in the overlap region in order to improve the device characteristics.

Note that the claimed limitations do not require the remaining oxide layer portions to extend outwardly from both the first and second leading edges of the gate structure. This allows the first overlap region to include a portion of the oxide layer which is not located beneath the gate structure.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Wieczorek et al. (6,352,885). Wieczorek et al. teach in figure 2E and related text a circuit structure comprising a semiconductor layer 101; a source region and a drain region 120, 130 in the semiconductor layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions;

an oxide layer 105, 125 formed on the semiconductor layer,

a gate electrode 104 formed on a portion of the oxide layer and having first and second leading edges, and

where a portion of the oxide layer defines a first overlap region 105 which is beneath the gate electrode and adjacent the first leading edge and inward of the second leading edge and a second overlap region of the oxide laver located beneath said gate structure and adjacent said first overlap region and said second leading edge and adjacent the drain region, the overlap region having an ion implant concentration higher than in said second overlap region 125 and all remaining oxide layer portions extending

outwardly from both the first and second leading edges of the gate structure, and which can be effective to lower the surface electrical field in the overlap region.

Wieczorek et al. do not explicitly state that the impurity concentration is sufficient to lower the surface electrical field in the overlap region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use sufficient impurity concentration in Wieczorek et al.'s device to lower the surface electrical field in the overlap region in order to improve the device characteristics.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 12-14, 46 and 48, insofar as in compliance with 35USC§112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram.

Akram teaches substantially the entire claimed structure, as applied to claim 3 above, except using a fluorine concentration of about 1 E 18 atoms per cubic centimeter.

Regarding claims 4, 13, 46 and 48, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a fluorine concentration of about 1 E 18 atoms per cubic centimeter in Akram's device, since it is within the skills of

an artisan in order to improve the characteristics of the device by routine experimentation and optimization.

Note that differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claims 12-14, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Akram's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. in view of Akram.

Wieczorek et al. teach substantially the entire claimed structure, as applied to claim 1 above, except using a fluorine concentration of about 1 E 18 atoms per cubic centimeter. Akram teaches using fluorine. It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to use a fluorine concentration of about 1 E 18 atoms per cubic centimeter in Wieczorek et al.'s device, in order to increase the effective gate thickness of the device and since it is within the skills of an artisan in order to improve the characteristics of the device by routine experimentation and optimization.

5. Claims 10 and 54, insofar as in compliance with 35USC§112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Admitted Prior Art (APA).

Akram teaches substantially the entire claimed structure, as applied to claim 3 above, except a gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer. APA teaches in figure 1 a gate electrode is comprised of a layer of polysilicon 18, a layer of titanium nitride 20 deposited on the polysilicon layer, and a layer of tungsten 22 deposited on the titanium layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode comprising of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer in Akram's device, in order to reduce the contact resistance of the device.

6. Claims 11-14 and 56-57, insofar as in compliance with 35USC§112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (5,750,435) in view of Motoyoshi et al. (JP 6-53492).

Akram teaches substantially the entire claimed structure, as applied to claim 3 above, except using the transistor in a CMOS configuration.

Motoyoshi et al. use a transistor having a gate oxide comprising fluorine in a CMOS configuration. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Akram's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

Regarding claims 11 and 57, Motoyoshi et al. teach in figure 7 a pair of conductive studs and an interlevel dielectric layer provided on the semiconductive layer, the interlevel dielectric layer have a pair of through holes, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a pair of conductive studs through an interlevel dielectric layer provided on the semiconductive layer, the interlevel dielectric layer have a pair of through holes, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions in Akram's device in order to operate the device in its intended use. Note that the device would not operate without external connections.

Regarding claim 13, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a fluorine concentration of about 1 E 18 atoms per cubic centimeter in Akram's device, since it is within the skills of an artisan in order to improve the characteristics of the device by routine experimentation and optimization. Note that differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele ,406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 56, Motoyoshi et al. teach in figure 7 source and drain regions having first and second dopants 17, 20, wherein the second dopant extending deeper into the semiconductor layer than the first dopant. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use source and drain regions having first and second dopants, wherein the second dopant extending deeper into the semiconductor layer than the first dopant in Akram's device in order to improve the characteristics of the device by introducing LDD regions.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference B is cited as being related to a gate oxide comprising higher impurity concentration.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such

papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
August 3, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800